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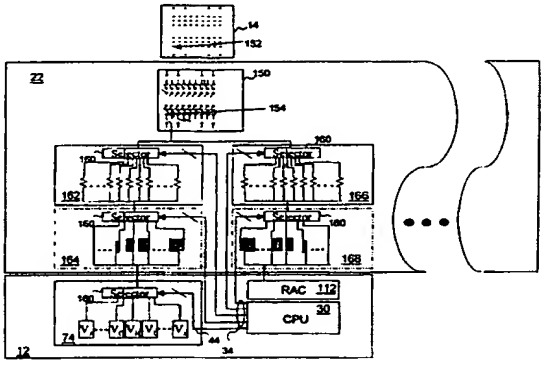

(57) Abstract: A tester comprises test logic and a connector for at least one device under test. The connector, which may comprise a wafer probe for dice on a wafer or a test fixture for packaged integrated circuit devices, has connections for the device under test that present an impedance selected to emulate the characteristic impedance of an end-use environment of the device under test. For example, in an embodiment in which the device under test comprises Rambus memory and the end-use environment is a Rambus channel, the characteristic impedance is between approximately 20 and 60 ohms. If, on the other hand, the end-use environment is a Rambus memory module, then the characteristic impedance is approximately 28 ohms. Thus, the tester of the present invention can accurately simulate operational behavior in an end-use environment of the device under test. Because this accurate simulation is available even for dice on a wafer, the needless expense associated with packaging defective dies and assembling defective dies into modules can be avoided. The test logic, which is coupled to the connector for communication with the device under test, transfers test commands and test data to the device under test. The test data and commands are utilized to perform multiples types of tests, including tests of the core logic and interface logic of the device under test. In this manner, the need for multiple types of testers is reduced or eliminated.

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METHOD AND SYSTEM FOR WAFER AND DEVICE-LEVEL TESTING OF AN INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

1. Technical Field:

The present invention relates in general to testing electronic devices and, in particular, to testing integrated circuits. Still more particularly, the present invention relates to a method and system for wafer and device-level testing of integrated circuits such as memories.

2. Description of the Related Art:

Integrated circuit memories, such as dynamic random access memories (DRAMs), are nearly universally utilized to provide data storage in electronic systems, such as computer systems. To ensure proper operation of the electronic systems, the manufacturing process for integrated circuit memories includes a number of testing steps intended to verify that the integrated circuit memories will provide reliable performance over the expected lifetime of the electronic systems in which they are installed.

A typical manufacturing process for DRAMs begins with the fabrication of a semiconductor wafer containing hundreds or even thousands of identical dice that each include integrated memory circuitry. The integrated memory circuitry in each die generally includes a memory array for storing data and may include interface circuitry for accessing the memory array and performing other operations in response to memory requests or commands.

Following wafer fabrication, a quick first pass wafer probe is performed in an attempt to identify dies on the wafer having defects. The first pass wafer probe, which is conventionally performed utilizing clock, address and data signals having lower than normal operating frequencies, writes and reads some or all memory

locations to identify defective rows and columns in the memory array.

Because memory array defects are not uncommon, a typical DRAM die is fabricated with one or more redundant rows and columns that can be activated in place of defective rows and columns by redundancy fusing. Thus, if any defects are detected during the first pass wafer probe, redundancy fusing is performed (e.g., by application of high voltage or lasing) to repair the defects. Once any such redundancy fusing has been performed, the wafer is subjected to a second pass wafer probe to determine the efficacy of fusing in addressing detected defects, and any dies failing the second pass wafer probe are marked as faulty.

Following the second pass wafer probe, the wafer is scribed into dice. Dice marked as faulty after the wafer probes are discarded, and dice passing the wafer probes are packaged to obtain DRAM devices. Packaging technologies that are commonly used for DRAMs include, among others, ball grid array (BGA) and wire bond.

After packaging, the packaged DRAMs are subjected to device-level testing. Device-level testing, like the wafer probe tests, may include low frequency tests of the DRAM array. Device-level testing may also include a "burn-in" test in which the packaged DRAMs under test are subjected to high ambient temperatures and tests of long duration in order to discover early life failures. Device-level testing also differs from wafer probe testing in that, in addition to basic pattern testing of memory arrays, device-level testing generally tests the DC and AC characteristics of the packaged DRAMs and the logic and operation of the memory interface. Device-level testing also differs from wafer probe testing in that device-level testing is typically performed at or near the rated signal frequencies of the packaged DRAM, which generally requires more sophisticated and expensive test equipment.

Packaged DRAMs that pass the device-level test may subsequently be assembled together on circuit cards to form memory modules such as SIMMs (single in-line memory modules) and DIMMs (dual in-line memory modules). Each memory module is then typically subjected to a final, intensive fault test prior to shipping or

installation. The faults detected by module testing include faults in the circuit cards themselves (e.g., open or shorted traces), faults introduced by module assembly (e.g., damaged pin drivers, open or shorted pins, and ESD damage), and undetected faults in the DRAM circuitry. Following completion of testing, DRAM devices and modules that pass can then be installed in an end-use application.

One drawback of the conventional DRAM manufacturing process outlined above is that a number of faults are not discovered until late in the manufacturing process, for example, during device-level and module testing. As appreciated by the present invention, if such defects could be detected earlier in the manufacturing process (i.e., during wafer testing), the significant expense associated with packaging and module assembly of the defective dice could be eliminated. Unfortunately, the expense of the sophisticated test equipment currently required to fully exercise integrated memory circuitry prohibits its use during wafer testing.

A second drawback of the conventional manufacturing process is that several different pieces of specialized test equipment are required to fully test many integrated circuits. For example, to test the memory array of a DRAM, an algorithmic tester is utilized to write a predetermined data pattern into the memory array, read out the contents of the memory array, and then compare the output data with the original data pattern. A separate vector tester is utilized to exercise the memory's interface logic. A third system tester is also employed to verify proper operation of the DRAM in response to commands. As will be appreciated, the use of multiple testers compounds the expense of testing.

A third drawback of the prior art is that conventional test equipment does not fully emulate the intended end-use environment of devices under test. In particular, conventional testers for packaged DRAM devices and modules have a fixed input impedance. This input impedance cannot be adjusted and may result in test behavior that is quite different from the operating behavior of the DRAM device under test when it is eventually installed in an end-use environment. Consequently, there may be an unacceptably high number of faulty devices or modules that pass the test process and even some satisfactory devices that fail the test process.

SUMMARY OF THE INVENTION

The present invention overcomes the foregoing and additional shortcomings in the prior art by introducing an improved method and system for wafer and device-level testing of integrated circuits such as integrated circuit memories.

According to a preferred embodiment of the present invention, a tester comprises test logic and a connector for at least one device under test. The connector, which may comprise a wafer probe for dice on a wafer or a test fixture for packaged integrated circuit devices, has connections for the device under test that present an impedance selected to emulate the characteristic impedance of an end-use environment of the device under test. For example, in an embodiment in which the device under test comprises Rambus™ memory and the end-use environment is a Rambus™ channel, the characteristic impedance is between approximately 20 and 60 ohms. If, on the other hand, the end-use environment is a Rambus™ memory module, then the characteristic impedance is approximately 28 ohms. Thus, the tester of the present invention can accurately simulate operational behavior in an end-use environment of the device under test. Because this accurate simulation is available even for dice on a wafer, the needless expense associated with packaging defective dies and assembling defective dies into modules can be avoided.

The test logic, which is coupled to the connector for communication with the device under test, transfers test commands and test data to the device under test. The test data and commands are utilized to perform multiples types of tests, including tests of the core logic and interface logic of the device under test. In this manner, the need for multiple types of testers is reduced or eliminated.

Additional objects, features, and advantages of the present invention will become apparent from the following detailed written description.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a high-level block diagram of a memory tester in accordance with a preferred embodiment of the present invention;

Figure 2 is a more detailed block diagram of a tester logic card in the memory tester illustrated in **Figure 1**;

Figure 3 depicts a portion of a wafer probe or test fixture for packaged devices having selectable termination impedance and propagation delay in accordance with a preferred embodiment of the present invention;

Figure 4 is a high level flowchart of an exemplary test process for testing Rambus™ memory in accordance with the present invention;

Figure 5A is a timing diagram illustrating the timing of the clock from master (CFM) and clock from master negative (CFMN) signals provided to Rambus™ memory under test in relation to the setup and hold times of the Rambus™ memory;

Figure 5B is a timing diagram depicting the use of a programmable delay in the clock from master (CFM) and clock from master negative (CFMN) signals provided to Rambus™ memory under test to test the timing sensitivity of WRITE operations;

Figure 6A is a timing diagram illustrating the timing of the clock to master (CTM) and clock to master negative (CTMN) signals provided by Rambus™ memory under test in relation to the valid times for sampling Rambus™ memory output pins;

Figure 6B is a timing diagram depicting the use of a programmable delay in the clock to master (CTM) and clock to master negative (CTMN) signals provided by Rambus™ memory under test to test the timing sensitivity of READ operations; and

Figure 7 illustrates an alternative embodiment of a memory tester in accordance with the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

With reference now to the figures and in particular with reference to **Figure 1**, there is depicted a high-level block diagram of an illustrative embodiment of a memory tester in accordance with the present invention. As illustrated, memory tester **10** includes one or more (e.g., 64) tester logic boards **12** that each includes circuitry for testing one device under test **14**. In the context of the present invention, a "device under test" (DUT) is defined as either a die on a semiconductor wafer or a packaged integrated circuit device. Each tester logic board **12** is coupled to a host **16** and a power source **18** (e.g., 110 V AC) via a communication bus **20** and a power bus **22**, respectively. Host **16**, which may be a suitably programmed personal computer or a control processor, downloads test procedures and test parameters to and receives test results from tester logic boards **12** via communication bus **20**.

As further illustrated in **Figure 1**, each tester logic board **12** is coupled to a respective DUT **14** by a controlled impedance connector **24** having connection elements suitable for the type of DUT **14** being tested. Thus, if DUTs **14** are memory dice on a wafer, connector **24** comprises a wafer probe; if, however, DUTs **14** are packaged memory devices, connector **24** comprises a test fixture having sites for connecting to packaged memory devices. For flexibility, tester logic boards **12** preferably employ a "universal" interface that can support both types of connectors **24**. Importantly, and as discussed further below, the connection elements of connector **24** present to each DUT **14** a characteristic impedance that is selected to simulate an end-use environment of DUTs **14**.

Referring now to **Figure 2**, there is illustrated a more detailed block diagram of a tester logic board **12** from **Figure 1** in accordance with a preferred embodiment of the present invention. The depicted embodiment includes circuitry specifically designed for testing Rambus™ dynamic random access memory (RDRAM) either on wafer or as packaged devices; however, those skilled in the art will appreciate that the present invention is not limited to RDRAM testing, but is instead applicable to testing other types of integrated circuitry. References useful for an understanding of the depicted embodiment of the present invention include the following Rambus™ documentation (which is incorporated herein by reference):

a) *Direct Rambus™ System and Board Design Considerations*, Rambus™, Inc., May 1998;
b) *RIMM Module Specification*, ver. 1.00, Rambus™, Inc.;
c) *128/144-Mbit Direct RDRAM Data Sheet*, Rev. 1.11, Rambus™, Inc., June 2000;
d) *RIMM Module Design Guide*, ver. 0.90, Rambus™, Inc.;
e) *Rambus RIMM Module (with 128/144-Mbit RDRAMs)*, Rev. 1.2, Rambus™, Inc., October 2000;
f) *Direct Rambus™ RAC*, rev. 1.11, Rambus™, Inc., July 24, 2000; and
g) *Direct Rambus™ Clock Generator Data Sheet*, Rev. 1.1, Rambus™, Inc., June 2000.

As shown, each tester logic board **12** includes a central processing unit (CPU) **30** that controls the testing performed by that tester logic board **12**. CPU **30** receives test procedures, test parameters, test data and expected test results from host **16** via communication bus **20** and communication interface **32**. Based upon these inputs, CPU **30** generates a number of output signals **34-44** (described further below) to orchestrate the operation of the other components of tester logic board **12** during testing.

In addition to CPU **30**, tester logic board **12** includes at least three principal subsystems: cooling subsystem **48**, tester logic **50** and power subsystem **52**. Cooling subsystem **48**, which may comprise, for example, a convection or thermoelectric cooling system, dissipates heat produced by the components of tester logic board **12**. The operation of cooling subsystem **48** is actively controlled by cooling control signals generated by thermal control logic **56** within tester logic **50** in response to the output of a thermal sensor **58**.

Power subsystem **52** includes a power supply **70** that utilizes power received from power bus **22** to provide power with the appropriate voltage and current characteristics to CPU **30** and tester logic **50**. Power subsystem **52** further includes a number of variable voltage supplies **72-78** that provide voltages utilized to operate DUT **14**. In the illustrated embodiment, in which tester logic board **12** is designed to test Rambus™ memory, variable power supplies **72-78** include variable reference voltage (V_{REF}) supply **72**, variable termination voltage (V_{TERM}) supply **74**, variable V_{DD} supply **76** and variable V_{DDA} supply **78**. Each of variable voltage sources **72-78** outputs a respective selected voltage specified by voltage select signals **44** provided by CPU **30**.

Power subsystem **52** finally includes at number of power measurement unit (PMUs) **80**, which are selectively coupled to the output pins of DUT **14** by relays **92**. Relays **92** can be configured by CPU **30** to route signals present at the output pins of DUT **14** either to tester logic **50** for evaluation of the correctness of their logic states and/or timing or to PMUs **80** for measurement of their DC power characteristics. As described further below, at least one of PMUs **80** measures the source voltage(s) and current supplied to DUT **14** by determining the voltage drop of V_{DD} across a test resistor **90**. Other PMUs **80** preferably measure the leakage current of the output pins of DUT **14**.

In addition to the thermal sensor **58** and thermal control logic **56** discussed above, tester logic **50** includes a sequencer **100**, which may comprise a general-purpose processor, a plurality of bit-slice (e.g., 4-bit) processors working in concert, or an application-specific integrated circuit (ASIC). Sequencer **100** is coupled to CPU **30** by a communication interface **102** through which sequencer **100** receives test parameters, test data, correct test results, and test procedures, which are stored by sequencer **100** in random access memory (RAM) **104**. Sequencer **100** also receives a reset signal **36** that, when asserted by CPU **30**, causes sequencer **100** to reset itself to a known stable state by reference to configuration parameters stored within non-volatile random access memory (NVRAM) **106**. The operation of sequencer **100** is timed by a clock **108**, which may be asynchronous the clocks utilized to operate DUT **14**.

Sequencer **100** is further connected to a memory controller **110**, which controls DUT **14** through a Rambus™ ASIC cell (RAC) **112** that is coupled to DUT **14** by relays **92** and connector **22**. The depicted arrangement of sequencer **100**, memory controller **110**, RAC **112**, connector **22** and DUT **114** simulates the memory subsystem of a personal computer system or other end-use environment of DUT **14**. That is, sequencer **100**, much like the CPU of a computer system, issues commands and requests to memory controller **110**, which can be implemented as a conventional complementary metal-oxide-semiconductor (CMOS) memory controller. Memory controller **110**, in turn, communicates with RAC **112** the commands and requests output by sequencer **100** and corresponding responses by DUT **14** utilizing conventional CMOS-level signaling. RAC **112** converts commands, requests, and responses between the lower-speed CMOS-level signals utilized by memory controller **110** and the high-speed Rambus™ Signal Level

(RSL) or Quad RSL (QRSL) signaling employed by DUT **14**. In addition, RAC **112** functions as a high performance parallel-to-serial and serial-to-parallel converter by packing and unpacking data packets communicated with memory controller **110** to and from wider Rambus™ data words.

During testing, sequencer **100** sets AC test parametrics for DUT **14**, initiates READ and WRITE data transfers to and from DUT **14**, and issues commands for DUT **14** based upon the test information stored in RAM **104**. In response to receipt of test results from DUT **14**, sequencer **100** logs the test results in RAM **104** and compares the test results with correct results also stored in RAM **104** to make a pass/fail determination for DUT **14**.

As further shown in **Figure 2**, communication between RAC **112** and DUT **14** is synchronized by a number of sets of clock signals including transfer clocks **120**, which are received by RAC **112** and DUT **14**. Transfer clocks **120** are selected by selector **124** from among a plurality of clock signals generated by clock sources **122** in response to a clock select signal **38** output by CPU **30**. The sets of clock signals utilized to synchronize communication with DUT **14** also include also include clock to master (CTM) clocks **130** generated by DUT **14** and clock from master (CFM) clocks **132** generated by RAC **112**. In order to test the timing sensitivity of DUT **14**, CTM clocks **130** and CFM clocks **132** each are passed through a respective one of programmable delays **134** and **136**, which applies a delay specified by a respective one of tester logic (TL) delay signal **40** and DUT delay signal **42**. Delays **134** and **136** each may be implemented, for example, with a Semtech Edge629 delay circuit and associated Semtech Edge693 driver circuit.

With reference now to **Figure 3**, a detailed depiction of a preferred embodiment of connector **22** from **Figures 1** and **2** is given. The illustrated embodiment includes a plurality of sites **150** (only one of which is shown), each of which has connections corresponding to the pinout of a DUT **14**. For example, the illustrated DUT **14** is a RDRAM device packaged in a micro-BGA package having a center-bonded layout of 54 pads **152**. Accordingly, site **150** has 54 connections **154**, each corresponding to a respective one of pads **152**. In a preferred embodiment, each connection **154** comprises a spring contact, such as a Microspring™ interconnection element produced by FormFactor.

Inc., of Livermore, California.

Although the interconnection of only one connection **154** of site **150** is shown in **Figure 3** for clarity, each connection **154** of a site **150** forms one point of a three-point circuit having RAC **112** and variable V_{TERM} supply **74** as termination points. As noted above, variable V_{TERM} supply **74** can produce a plurality of different termination voltages (represented by voltages V_A-V_Z), only one of which is selected by a selector **160** to be the termination voltage V_{TERM} in response to voltage select signals **44** provided by CPU **30**.

Between each connection **154** and each of variable V_{TERM} supply **74** and RAC **112**, an impedance and an optional propagation delay element are connected in the signal path. That is, a termination impedance **162** and an optional first propagation delay element **164** are coupled between connection **154** and variable V_{TERM} supply **74**, and a test impedance **166** and an optional second propagation delay element **168** are coupled between connection **154** and RAC **112**. In accordance with an important aspect of the present invention, the input impedance presented by each connection **154** of site **150**, which is the sum of the contact impedance of connection **154** plus the parallel combination of termination impedance **162** and test impedance **166**, is equivalent to the characteristic impedance of an end-use environment of DUT **14**. For example, if the end-use environment is a Direct Rambus™ module, such as a Rambus™ In-line Memory Module (RIMM), Small Outline RIMM (SO-RIMM) or Media RIMM, the characteristic impedance is selected to be approximately 28 Ω, and more particularly, 28 Ω ± 10%. If, on the other hand, the end-use environment is a Direct Rambus™ channel, the characteristic impedance is selected to be between 20 and 60 Ω. As shown, in a preferred embodiment, multiple end-use environments can be emulated and non-standard impedances outside of specified tolerances can be supported by implementing termination impedance **162** and test impedance **166** as variable impedances. In this preferred embodiment, a respective selector **160** selects impedances **162** and **166** from among a plurality of different impedances in response to select signals **34** provided by CPU **30**.

Optional propagation delay elements **164** and **168** can be employed to test the timing sensitivity of DUT **14** to various propagation delays that result, for example, from different installation locations of DUT **14** on the Rambus™ channel. As illustrated, the

operational effects of introducing various different propagation delays into the signal path between connector **154** and variable V_{TERM} supply **74** or the signal path between connector **154** and RAC **112** can be tested through selection of trace run lengths by selectors **160** of propagation delay elements **164** and **168**. As with impedances **162** and **166**, the select signals **34** that control selectors **160** of propagation delay elements **164** and **168** are supplied by CPU **30**. In an alternative embodiment of the present invention, the installation of DUT **14** at various locations on the Rambus™ channel can be simulated by including within connector **22** a series of dummy packaged devices that can be connected to the Rambus™ channel in a selectable order relative to DUT **14**. In this manner, testing can simulate the installation of DUT **14** as the device closest to RAC **112**, second closest to RAC **112**, etc.

With reference now to **Figure 4**, there is illustrated a high-level logical flowchart of an exemplary test process for testing Rambus™ memory, either on wafer or in packaged RDRAM devices, utilizing tester **10** from **Figure 1**. As illustrated, the process begins at block **180** and then proceeds to block **182**, which depicts tester **12** performing DC parametric tests upon a DUT **14** while the DUT **14** is idle. To perform the DC parametric tests, CPU **30** sets relays **92** to connect the output pins of DUT **14** to PMUs **80** rather than RAC **112**. PMUs **80** then measure the power dissipation of DUT **14** for one or more sets of V_{REF}, V_{DD} and V_{DDA} voltages. In addition, PMUs **80** measure the leakage current of the pins of DUT **14**. These power and current measurements are then transferred to sequencer **100** via unillustrated connections for storage in RAM **104** and comparison with acceptable values to obtain a pass/fail determination.

The process then proceeds from block **182** to block **184**, which illustrates CPU **30** setting the AC parameters to be utilized during the Rambus™ interface testing illustrated at block **186**, which is described below. As represented by decision block **188**, Rambus™ interface testing (and each of the other AC tests) is preferably performed with multiple different sets of AC parameters in order to assess the proper operation of DUT **14** over a wide range of AC parameters. For DUTs **14**, which comprise Rambus™ memory, the AC parameters that can be varied during AC testing include those summarized below in Table I. Of course, for different DUTs, other or additional AC parameters can be tested.

TABLE I

AC parameter	Description
T_{CYCLE}	transfer clock frequency
T_{SH}	combined setup and hold times for DUT (i.e., period defining valid WRITE data)
T_Q	time to valid data output (i.e., period defining valid READ data)
T_{TR}	time from transmit to receive (i.e., interval between consecutive READ and WRITE operations)
V_{REF}	reference voltage that defines midpoint between the logic low input voltage (V_{IL}) and logic high input voltage (V_{IH})
V_{TERM}	termination voltage for Rambus™ channel

CPU **30** sets the T_{CYCLE} parameter by generating appropriate clock selects **38** to select a clock source **122** of a desired frequency to supply transfer clock **120**. In a typical testing scenario, it is desirable to select clock frequencies below, at, and above the rated clock frequency of DUT **14**. For example, for a Rambus™ DUT **14** having a rated clock frequency of 533 MHz, it is desirable to performing testing at a number of transfer clock frequencies ranging from approximately 300 MHZ to approximately 550 MHz.

In order to test the sensitivity of DUT **14** to the timing of WRITE operations, CPU **30** sets the T_{SH} parameter by generating a DUT delay signal **42** to select the delay applied by delay **136** to the clock from master (CFM) and the complementary clock from master negative (CFMN) signals **132** output to DUT **14** by RAC **112**. As illustrated in **Figure 5A**, which illustrates signal timing without any delay, the high-to-low crossing of CFM with CFMN defines a timing of a valid period during which data (e.g., ROW, COL, DQA and DQB) and commands are sampled by DUT **14**. The extent of the valid period is equal to the sum of a setup time (t_S) prior to the crossing of CFM and CTMN during which the data and commands must be valid and a hold time (t_H) following the crossing of CFM and CFMN during which the commands must be stable. As shown in **Figure 5B**, the sensitivity of DUT **14** to variations in WRITE timing can be tested by applying a delay to CFM and CFMN equal to a full cycle minus Δt_1. By doing so, the setup time (t_S) is effectively decreased by Δt_1, and the timing sensitivity of DUT **14** can be evaluated.

CPU **30** similarly tests the timing sensitivity of DUT **14** during READ operations

by setting the T_Q parameter through generation of TL delay signal **40** that selects a delay applied to the clock to master (CTM) and complementary clock to master negative (CTMN) signals **130** by delay **134**. As illustrated in **Figure 6A**, which depicts signal timing without any applied delay, the high-to-low crossing of CTM with CTMN defines a timing of a period (t_Q) during which data (i.e., DQA and DQB) read out of DUT **14** are valid for sampling by RAC **112**. The extent of the valid period t_Q is equal to the period of CTM minus the two intervals $t_{Q,MIN}$ and $t_{Q,MAX}$. As shown in **Figure 5B**, the sensitivity of DUT **14** to variations in READ timing can be tested by applying a delay to CTM and CTMN equal to a full cycle minus Δt_2. By doing so, the valid period (t_Q) is effectively decreased by Δt_2, and the timing sensitivity of DUT **14** can be evaluated.

CPU **30** tests the T_{TR} parameter by shifting the phase of CTM/CTMN relative to CFM/CFMN utilizing appropriate delay signals **40** and **42**. By varying the relative timing of these clock signal pairs by small increments, CPU **30** can test DUT **14** for worst-case failures for consecutive READ and WRITE operations.

V_{REF} and V_{TERM} are set by CPU **30** utilizing voltage select signals **44** in order to test DUT **14** for supply voltage margin and launch voltage sensitivity, respectively. Because DUT **14** calibrates V_{IL} and V_{IH} to V_{REF}, varying V_{REF} also tests the sensitivity of DUT **14** to various input voltage levels without the need to actually vary the voltage levels of the data inputs provided to DUT **14**.

Referring again to **Figure 4**, after the AC parameters are set at block **184**, CPU **30** downloads vector data and correct test results to sequencer **100**, which stores them in RAM **104**. Sequencer **100** utilizes the vector data to stimulate appropriate input pins of DUT **14** to exercise the Rambus™ interface of DUT **14**. In addition, sequencer **100** tests the sensitivity of DUT **14** to the timing of READ and WRITE operations and to failure due to insufficient output buffer launch voltage.

Failures due to insufficient output buffer launch voltage are discovered by performing multiple READ operations back-to-back to locations in the memory arrays of DUT **14** that share the same output buffer. By repeatedly reading from memory locations sharing the same output buffer, charge can be depleted from the output buffer, and failure

can occur because the launch voltage is too weak to overcome reflected signals from prior transactions on the Rambus™ channel. The probability of failure during testing can be increased or decreased by:

(1) varying termination impedance **162** and test impedance **166** while maintaining the characteristic impedance of an end-use environment or varying the impedance from the characteristic impedance of the end-use environment in order to affect the amplitude of the Rambus™ channel reflections; and/or

(2) varying the delay applied by delay elements **164** and **168** to simulate different locations of DUT **14** on the Rambus™ channel, which affects the timing of reflections on the Rambus™ channel relative to the output of DUT **14**; and/or

(3) varying V_{TERM} either above or below the standard value of 1.8 ± 0.1V.

If failure due to insufficient output buffer launch voltage is observed, CPU **30** preferably determines if the failing DUT **14** can pass the test under simulated work-around conditions. The work-around conditions can be simulated, for example, by applying only certain signal propagation delays with delay elements **164** and **168** in order to simulate restricting the installation locations for DUT **14** along the Rambus™ channel, by setting V_{TERM} above 1.9 V, and by changing the characteristic impedance to a value outside of the specified ranges for module and non-module systems. If repeating the output buffer launch voltage test with simulated work-around conditions results in an originally failing DUT **14** passing the test, the failing DUT **14** can be reclassified as a conditionally passing subject to the work-around conditions.

Sequencer **100** logs the results of the Rambus™ interface test and compares the test results with the correct results to produce a pass/fail determination. As illustrated at block **188**, CPU **30** may then alter the AC parameters and repeat the Rambus™ interface test utilizing the new AC parameters.

If Rambus™ interface testing has been performed utilizing each desired set of AC parameters, then the process proceeds to block **190**, which depicts CPU **30** setting initial AC parameters for Rambus™ channel packet testing. CPU **30** then downloads a Rambus™ channel command set and correct results to sequencer **100**, which stores them

in RAM **104**. As shown at block **192**, sequencer **100** transfers the Rambus™ channel commands to DUT **14**, logs responses of DUT **14** to the channel commands in a test log in RAM **104**, and compares the responses with the correct results to make a pass/fail determination. Following block **192**, the process proceeds to block **194**, which represents CPU **30** causing sequencer **100** to repeat the Rambus™ channel packet test for each desired set of AC parameters.

The process illustrated in **Figure 4** next proceeds to block **196**, which shows CPU **30** establishing initial AC parameters for Rambus™ core testing. CPU **30** also downloads to sequencer **100** a set of data patterns to be written into and read from the memory arrays of DUT **14**. Sequencer **100** stores the data patterns in RAM **104**, and as depicted at block **198**, issues WRITE and READ operations to DUT **14** to verify correct operation of the memory arrays of DUT **14**. A typical core test suite for DUT **14** can include the individual tests summarized below in Table III.

TABLE III

Rambus™ core test suite tests	Description
Address	ensures that all memory array locations can be accessed
Data	verifies that each memory bit operates as both a 1 and a 0
Refresh	memory array properly retains data
March algorithms	data patterns written into memory arrays match those read out of memory arrays
Disturb Neighborhood Sensitivity Test (DNST)	modifying contents of a memory cell in the memory array does not modify data stored in neighboring memory cells

Data received from DUT **14** in response to READ accesses are compared with the expected data pattern by sequencer **100** to make a pass/fail determination for DUT **14**. As illustrated at block **200**, CPU **30** may instruct sequencer **100** to perform tests in the Rambus™ core test suite utilizing a number of additional AC parameter sets.

As shown at blocks **202-206**, CPU **30** may also perform additional Rambus™ functional tests that verify special functionality of Rambus™ memory. A number of these

Rambus™ functional tests are summarized below in Table IV.

TABLE IV

Rambus™ functional tests	Description
Bank interleave	verify bank addressing of all memory banks
Write/Retire	checks operation of write retire buffer
Byte Operation Mask	verifies operation of mask programmed via the Rambus™ COLM bus
NAP and Power Down	assures operation in low-power modes

After the Rambus™ functional tests are performed for all desired sets of AC parameters, the test process ends at block **210**, and sequencer **100** relays the pass/fail determinations to CPU **30**, which reports the pass/fail determinations for this DUT **14** to host **16**.

Referring now to **Figure 7**, there is depicted a high-level block diagram of a host-based memory tester **250** in accordance with an alternative embodiment of the present invention. In **Figure 7**, like reference numerals are utilized to identify elements that are the same as or similar to those of the memory tester embodiment illustrated in **Figures 1-3**.

As shown, memory tester **250** comprises a host **16'** and a tester logic board **254**. Host **16'**, which may comprise, for example, a conventional personal computer system or other data processing system, includes a system board **252** having an interconnect **258** to which a CPU **30**, memory controller **110**, and peripheral adapter **260** are coupled for communication. Memory controller **110** is coupled to RAC **112**, which is in turn connected to a standard Rambus™ memory module socket **256** mounted on system board **252**. Peripheral adapter **260** is coupled to a storage device **262**, which provides non-volatile storage for test procedures, test parameters, and test data.

Memory tester **250** employs a host-based tester architecture that permits CPU **30** of host **16'** to test a Rambus™ DUT **14** as if DUT **14** were mounted on a standard Rambus™ memory module through the installation, in socket **256**, of a tester logic board **254** having a impedance-controlled connector **22** for DUT **14**. Like tester logic board **12**

of **Figure 2**, tester logic board **254** includes a cooling subsystem **48** and a power subsystem **52**, as well as tester logic **50'**. In the alternative embodiment shown in **Figure 7**, tester logic **50'** is greatly simplified as compared to tester logic **50** of **Figure 2** in that no sequencer **100** is required and the memory controller **110** and RAC **112** utilized for testing are mounted on system board **252**. The one major addition to tester logic **50'** is a serial presence detect (SPD) emulation circuit **255** that identifies tester logic board **254** to host **16'** as a Rambus™ memory module upon system reset. Information regarding the operation of SPD emulation circuit **255** may be found, for example, in *Direct Rambus™ SPD Specification*, rev. 1.1, Rambus™, Inc., June 2000, which in incorporated herein by reference.

In operation, memory tester **250** utilizes the test information stored by storage device **262** (or remotely stored test information communicated via a network connection) to test DUT **14** according to the test process depicted in **Figure 4** and described above. The major difference in the manner in which testing is performed by the embodiment of **Figure 7** is that CPU **30** directly accesses DUT **14** as if DUT **14** were mounted on a Rambus™ memory module installed in socket **256**. Thus, for example, to write to or read from DUT **14**, CPU **30** issues an appropriate request on interconnect **258**, which memory controller **110** passes to RAC **112** utilizing CMOS signaling. In response to the request, RAC **112** issues a command to DUT **112** via socket **256** and connector **22**. Responses by DUT **14** to access commands are returned via the same path. CPU **30** can then compare the responses provided by DUT **14** with expected results to make pass/fail determinations for the various tests.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention. For example, although aspects of the present invention have been described with respect to a tester system executing software that directs the functions of the present invention, it should be understood that the present invention may alternatively be implemented as a program product for use with a data processing system. Programs defining the functions of the present invention can be delivered to a data processing system via a variety of signal-bearing media, which include, without limitation, non-rewritable storage

media (e.g., CD-ROM), rewritable storage media (e.g., a floppy diskette or hard disk drive), and communication media, such as digital and analog networks. It should be understood, therefore, that such signal-bearing media, when carrying or encoding computer readable instructions that direct the functions of the present invention, represent alternative embodiments of the present invention.

CLAIMS

What is claimed is:

1. A tester for testing dice on a wafer, said tester comprising:

a wafer probe card having connections for at least one die on a wafer, wherein the connections of the wafer probe card present an impedance selected to emulate the characteristic impedance of an end-use environment for a packaged device containing the at least one die; and

tester logic, coupled to the wafer probe card, that communicates test data with the at least one die on the wafer via the wafer probe card.

2. The tester of Claim 1, wherein the at least one die is a Rambus memory die, the end-use environment is a Rambus channel, and the characteristic impedance is between 20 and 60 ohms.

3. The tester of Claim 1, wherein the at least one die is a Rambus memory die, the end-use environment is a Rambus memory module, and the characteristic impedance is approximately 28 ohms.

4. The tester of Claim 1, wherein the connections comprise microsprings.

5. The tester of Claim 1, said wafer probe card including a variable impedance network having a dynamically alterable impedance selected by the tester logic.

6. The tester of Claim 1, wherein said wafer probe card includes at least one dummy

packaged device to simulate operating characteristics of the end-use environment.

7. The tester of Claim 1, wherein the at least one die comprises a memory die including memory cells, and wherein the tester logic includes means for communicating voltage signals to the memory die on the wafer to alter which memory cells in the memory die are active for operations to specific address locations.

8. The tester of Claim 1, wherein the tester logic includes a Rambus ASIC cell (RAC) that interfaces with the wafer probe card.

9. The tester of Claim 1, wherein the tester logic further comprises:

a clock generator that generates at least one clock signal received by the tester logic and at least one corresponding clock signal received by the at least one die on the wafer, wherein the at least one clock signal coordinates data transfer between the tester logic and the at least one die; and

one or more delay elements that selectively alter the relative phases of the at least one clock signal received by the at least one die and the at least one clock signal received by the tester logic in order to test timing sensitivity of the at least one die.

10. The tester of Claim 9, wherein the one or more delay elements delay the at least one clock signal sent to the at least one die relative to the corresponding at least one clock signal sent to the tester logic.

11. The tester of Claim 10, wherein the at least one die comprises a Rambus memory die, and wherein the at least one clock signal received by the Rambus memory die comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

12. The tester of Claim 11, wherein the tester logic outputs to the Rambus memory die data signals and row and column signals while the one or more delay elements delay the clock-from-master positive polarity clock signal (CFM) and the clock-from-master negative polarity (CFMN) clock signal to the Rambus memory die in order to test sensitivity of the Rambus memory die to the setup and hold timing parameters for writes to the Rambus memory die.

13. The tester of Claim 9, wherein the one or more delay elements delay the at least one clock signal sent to the tester logic relative to the corresponding at least one clock signal sent to the at least one die.

14. The tester of Claim 13, wherein the at least one die comprises a Rambus memory die, and wherein the at least one clock signal received by the Rambus memory die comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

15. The tester of Claim 14, wherein the tester logic receives data signals from the Rambus memory die while the one or more delay elements delay the clock-to-master (CTM) clock signal and the clock-to-master negative (CTMN) clock signal to the tester logic in order to test sensitivity of a clock-to-data output timing parameter for reads from the Rambus memory die.

16. The tester of Claim 9, wherein the one ore more delay elements shift the phase of the at least one clock signal received by the at least one die in small increments relative to the at least one clock signal received by the tester logic to vary the timing between reads from the at least one die and writes to the at least one die to test for worst case failures.

17. The tester of Claim 16, wherein:

the at least one die comprises a Rambus memory die;

the at least one clock signal received by the Rambus memory die comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal; and

the at least one clock signal received by the tester logic comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal.

18. The tester of Claim 1, wherein said at least one die includes an output buffer, and wherein the tester logic includes means for testing the sensitivity of the at least one die on the wafer to failure due to insufficient launch voltage of the output buffer.

19. The tester of Claim 18, wherein the at least one die comprises a Rambus memory die, and wherein the means for testing comprises means for testing the sensitivity of the Rambus memory die to insufficient launch voltage of the output buffer by issuing a plurality of sequential read operations targeting one or more memory locations that share the output buffer.

20. The tester of Claim 18, wherein:

the at least one die comprises a Rambus memory die;

the wafer probe card includes a variable termination voltage source for the connections; and

the means for testing comprises means for testing sensitivity of the Rambus memory die to insufficient launch voltage of the output buffer by setting the termination voltage provided by the variable termination voltage source outside of a predetermined termination voltage range.

21. The tester of Claim 18, wherein the wafer probe card comprises at least one delay element that delays one or more signals communicated with the at least one die to test sensitivity of the at least one die to insufficient launch voltage of the output buffer.

22. The tester of Claim 18, wherein:

the at least one die comprises a Rambus memory die;

the wafer probe card comprises at least one variable impedance representative of a characteristic impedance of a Rambus channel; and

the means for testing varies the variable impedance to test sensitivity of one or more Rambus memory dice to insufficient launch voltage of the output buffer.

23. The tester of Claim 22, wherein the at least one variable impedance comprises at least a first variable impedance and a second variable impedance, wherein the means for testing tests sensitivity of the Rambus memory die to insufficient launch voltage of the output buffer for various installed location on a Rambus channel by varying the first and second variable impedances to simulate different installed locations on a Rambus channel.

24. The tester of Claim 1, wherein:

the at least one die comprises a memory die; and

the tester logic comprises a tester logic interface to which a host system communicates memory access requests in order to access the memory die.

25. The tester of Claim 24, and further comprising the host system coupled to the tester logic interface, wherein the host system accesses the memory die on the wafer via the tester logic and wafer probe card by communicating memory access requests to the tester logic interface.

26. A tester for testing packaged integrated circuit devices, said tester comprising:

a test fixture having connections for at least one packaged integrated circuit device, wherein the connections of the test fixture present an impedance selected to emulate the characteristic impedance of an end-use environment for the at least one packaged integrated circuit device; and

tester logic, coupled to the test fixture, that communicates test data with the at least one packaged device via the test fixture.

27. The tester of Claim 26, wherein the at least one packaged integrated circuit device is a packaged Rambus memory device, the end-use environment is a Rambus channel, and the characteristic impedance is between 20 and 60 ohms.

28. The tester of Claim 26, wherein the at least one packaged integrated circuit device is a packaged Rambus memory device, the end-use environment is a Rambus memory module, and the characteristic impedance is approximately 28 ohms.

29. The tester of Claim 26, wherein the connections comprise microsprings.

30. The tester of Claim 26, said test fixture including a variable impedance network having a dynamically alterable impedance selected by the tester logic.

31. The tester of Claim 26, wherein said test fixture includes at least one dummy packaged integrated circuit device to simulate operating characteristics of the end-use

environment.

32. The tester of Claim 26, wherein the at least one packaged integrated circuit device comprises a packaged Rambus memory device, and wherein the tester logic includes a Rambus ASIC cell (RAC) that interfaces with the test fixture.

33. The tester of Claim 26, wherein the tester logic further comprises:

a clock generator that generates at least one clock signal received by the tester logic and at least one corresponding clock signal received by the at least one packaged integrated circuit device, wherein the at least one clock signal coordinates data transfer between the tester logic and the at least one packaged integrated circuit device; and

one or more delay elements that selectively alter the relative phases of the at least one clock signal received by the at least one packaged integrated circuit device and the at least one clock signal received by the tester logic in order to test timing sensitivity of the at least one packaged integrated circuit device.

34. The tester of Claim 33, wherein the one or more delay elements delay the at least one clock signal sent to the at least one packaged integrated circuit device relative to the corresponding at least one clock signal sent to the tester logic.

35. The tester of Claim 34, wherein the at least one packaged integrated circuit device comprises a packaged Rambus memory device, and wherein the at least one clock signal received by the packaged Rambus memory device comprises a clock-from-master

positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

36. The tester of Claim 35, wherein the tester logic outputs to the packaged Rambus memory device data signals and row and column signals while the one or more delay elements delay the clock-from-master positive polarity clock signal (CFM) and the clock-from-master negative polarity (CFMN) clock signal to the packaged Rambus memory device in order to test sensitivity of the packaged Rambus memory device to setup and hold timing parameters for writes to the packaged Rambus memory device.

37. The tester of Claim 33, wherein the one or more delay elements delay the at least one clock signal sent to the tester logic relative to the corresponding at least one clock signal sent to the at least one packaged integrated circuit device.

38. The tester of Claim 37, wherein the at least one packaged integrated circuit device comprises a packaged Rambus memory device, and wherein the at least one clock signal received by the packaged Rambus memory device comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal.

39. The tester of Claim 14, wherein the tester logic receives data signals from the packaged Rambus memory device while the one or more delay elements delay the clock-to-master (CTM) clock signal and the clock-to-master negative (CTMN) clock signal to the tester logic in order to test sensitivity of a clock-to-data output timing parameter for reads from the packaged Rambus memory device.

40. The tester of Claim 33, wherein the one ore more delay elements shift the phase of

the at least one clock signal received by the at least one packaged integrated circuit device in small increments relative to the at least one clock signal received by the tester logic to vary the timing between reads from the at least one packaged integrated circuit device and writes to the at least one packaged integrated circuit device to test for worst case failures.

41. The tester of Claim 40, wherein:

the at least one packaged integrated circuit device comprises a packaged Rambus memory device;

the at least one clock signal received by the packaged Rambus memory device comprises a clock-from-master positive polarity (CFM) clock signal and a clock-from-master negative polarity (CFMN) clock signal; and

the at least one clock signal received by the tester logic comprises a clock-to-master positive polarity (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal.

42. The tester of Claim 26, wherein said at least one packaged integrated circuit device includes an output buffer, and wherein the tester logic includes means for testing the sensitivity of the at least one packaged integrated circuit device to failure due to insufficient launch voltage of the output buffer.

43. The tester of Claim 42, wherein the at least one packaged integrated circuit device comprises a packaged Rambus memory device, and wherein the means for testing comprises means for testing the sensitivity of the packaged Rambus memory device to insufficient launch voltage of the output buffer by issuing a plurality of sequential read operations targeting one or more memory locations that share the output buffer.

44. The tester of Claim 42, wherein:

the at least one packaged integrated circuit device comprises a packaged Rambus memory device;

the test fixture includes a variable termination voltage source for the connections; and

the means for testing comprises means for testing sensitivity of the packaged Rambus memory device to insufficient launch voltage of the output buffer by setting the termination voltage provided by the variable termination voltage source outside of a predetermined termination voltage range.

45. The tester of Claim 42, wherein the test fixture comprises at least one delay element that delays one or more signals communicated with the at least one packaged integrated circuit device to test sensitivity of the at least one packaged integrated circuit device to insufficient launch voltage of the output buffer.

46. The tester of Claim 42, wherein:

the at least one packaged integrated circuit device comprises a packaged Rambus memory device;

the test fixture comprises at least one variable impedance representative of a characteristic impedance of a Rambus channel; and

the means for testing varies the variable impedance to test sensitivity of the packaged Rambus memory device to insufficient launch voltage of the output buffer.

47. The tester of Claim 46, wherein the at least one variable impedance comprises at least a first variable impedance and a second variable impedance, wherein the means for testing tests sensitivity of the packaged Rambus memory device to insufficient launch voltage of the output buffer for various installed location on a Rambus channel by varying the first and second variable impedances to simulate different installed locations on a Rambus channel.

48. The tester of Claim 26, wherein:

the at least one packaged integrated circuit device comprises a packaged integrated circuit memory; and

the tester logic comprises a tester logic interface to which a host system communicates memory access requests in order to access the packaged integrated circuit memory.

49. The tester of Claim 48, and further comprising the host system coupled to the tester logic interface, wherein the host system accesses the packaged integrated circuit memory device via the tester logic and test fixture by communicating memory access requests to the tester logic interface.

50. A memory tester, comprising:

a connector having connections for a memory that is one of a packaged integrated circuit device and a memory die on a wafer, wherein the connections of the apparatus present an impedance selected to emulate the characteristic impedance of an end-use environment for the at least one packaged integrated circuit device; and

tester logic, coupled to the apparatus, that communicates test data with the memory.

51. The memory tester of Claim 50, wherein the memory is one of a packaged Rambus Dynamic Random Access Memory (RDRAM) and a Rambus memory die, and wherein the end-use environment is one of a Rambus channel and a Rambus memory module.

52. A method of testing an integrated circuit device, said method comprising:

connecting a device under test that is one of a packaged integrated circuit device and a memory die on a wafer to connections of a connector, wherein the connections present an impedance selected to emulate the characteristic impedance of an end-use environment for a packaged integrated circuit device; and

coupling test logic to the connector;

communicating test data between the device under test and the test logic via the connector to test the device under test.

53. The method of Claim 52, wherein the at least one die is a Rambus memory die, the end-use environment is a Rambus channel, and the characteristic impedance is between 20 and 60 ohms.

54. The method of Claim 52, wherein the at least one die is a Rambus memory die, the end-use environment is a Rambus memory module, and the characteristic impedance is approximately 28 ohms.

55. The method of Claim 52, wherein said connector includes a variable impedance network, and wherein communicating test data between the device under test and the test logic comprises communicating test data with said variable impedance network set to multiple different impedances.

56. The method of Claim 1, wherein the at least one device under test includes memory cells, and wherein the method further comprises communicating voltage signals to the device under test to alter which memory cells are active for operations to specific address locations.

57. The method of Claim 52, and further comprising interfacing the connector to the tester logic with a Rambus ASIC cell (RAC).

58. The method of Claim 1, and further comprising:

generating at least one first clock signal received by the tester logic and at least one second clock signal received by the device under test, wherein the first and second clock signals coordinate data transfer between the tester logic and the device under test; and

selectively altering the phase of one of the first clock signal and the second clock signal to test timing sensitivity of the device under test.

59. The method of Claim 58, wherein selectively altering comprises delaying the second clock signal sent to the device under test.

60. The method of Claim 58, wherein the device under test comprises Rambus memory, and wherein generating at least one second clock signal comprises generating a clock-from-master (CFM) clock signal and a clock-from-master negative (CFMN) clock signal.

61. The method of Claim 60, wherein the tester logic outputs, to the device under test, data signals and row and column signals while the clock-from-master (CFM) clock signal and the clock-from-master negative (CFMN) clock signal are delayed in order to test sensitivity of the device under test to the setup and hold timing parameters for writes.

62. The method of Claim 58, wherein selectively altering comprises delaying the at least first one clock signal sent to the tester logic.

63. The method of Claim 62, wherein the at least one die comprises Rambus memory, and wherein the at least one first clock signal comprises a clock-to-master (CTM) clock signal and a clock-to-master negative polarity (CTMN) clock signal.

64. The method of Claim 63, wherein the tester logic receives data signals from the device under test while the clock-to-master (CTM) clock signal and the clock-to-master negative (CTMN) clock signal are delayed to test sensitivity of a clock-to-data output timing parameter for reads.

65. The method of Claim 58, wherein selectively altering comprises shifting the phase of the at least one second clock signal received by the device under test in increments relative to the at least one second clock signal received by the tester logic to vary the timing between reads from the device under test and writes to the device under test to test for worst case failures.

66. The method of Claim 52, wherein device under test includes an output buffer, and wherein the method further comprises testing the sensitivity of the device under test to

failure due to insufficient launch voltage of the output buffer.

67. The method of Claim 66, wherein testing the sensitivity of the device under test to failure due to insufficient launch voltage of the output buffer comprises testing the sensitivity of the device under test to insufficient launch voltage of the output buffer by issuing a plurality of sequential read operations targeting one or more memory locations in the device under test that share the output buffer.

68. The method of Claim 66, wherein testing the sensitivity of the device under test to failure due to insufficient launch voltage of the output buffer comprises testing sensitivity of the device under test to insufficient launch voltage of the output buffer by setting a termination voltage provided by a variable termination voltage source outside of a predetermined termination voltage range.

69. The method of Claim 66, wherein testing the sensitivity of the device under test to failure due to insufficient launch voltage of the output buffer comprises delaying one or more data signals communicated with the device under test.

70. The method of Claim 66, wherein testing the sensitivity of the device under test to failure due to insufficient launch voltage of the output buffer comprises varying at least one variable signal line impedance.

71. The method of Claim 70, wherein the at least one variable signal line impedance comprises a first variable impedance and a second variable impedance, and wherein varying the at least one signal line impedance comprises varying the first and second variable impedances to simulate different installed locations of the device under test on a

communication channel.

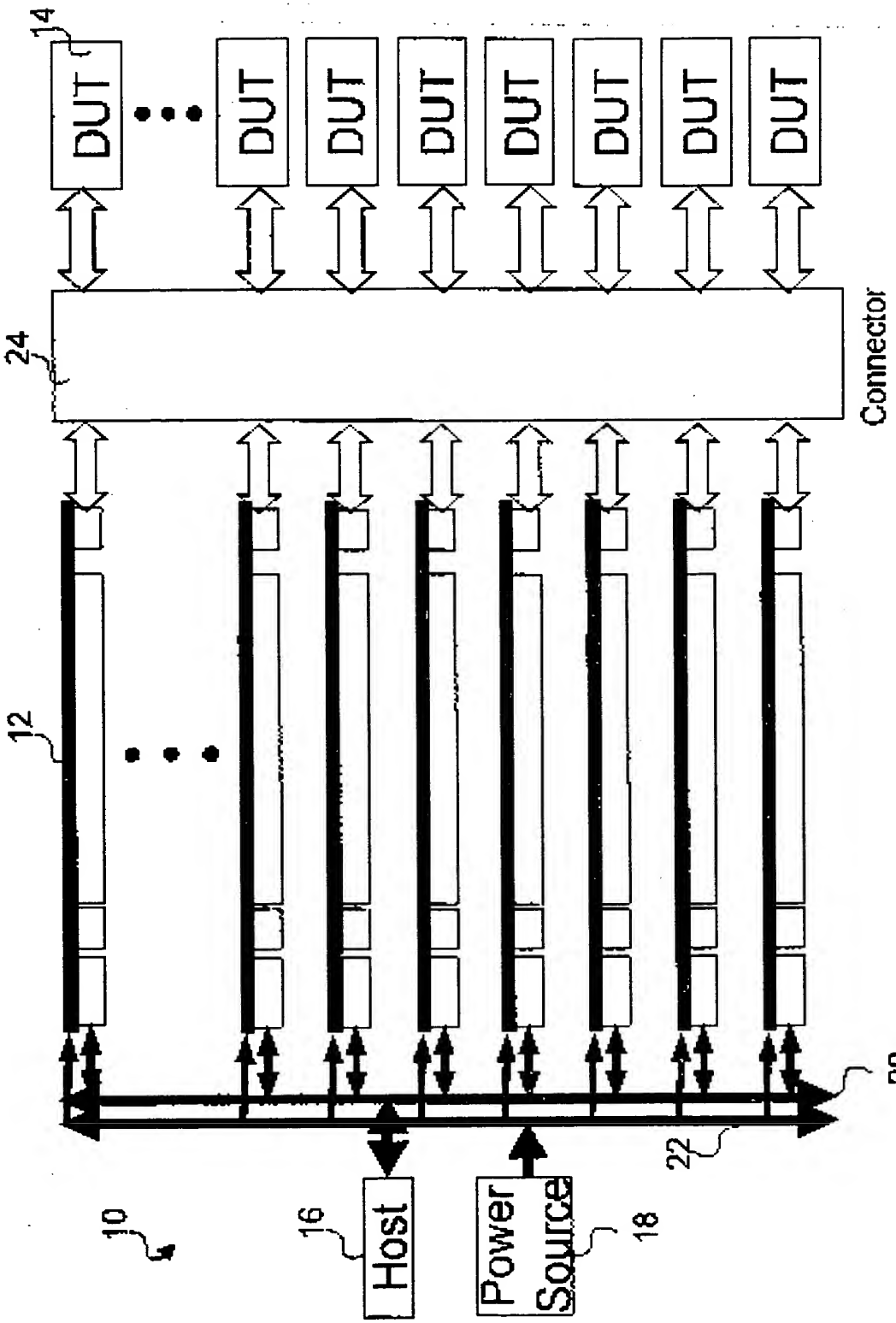

Figure 1

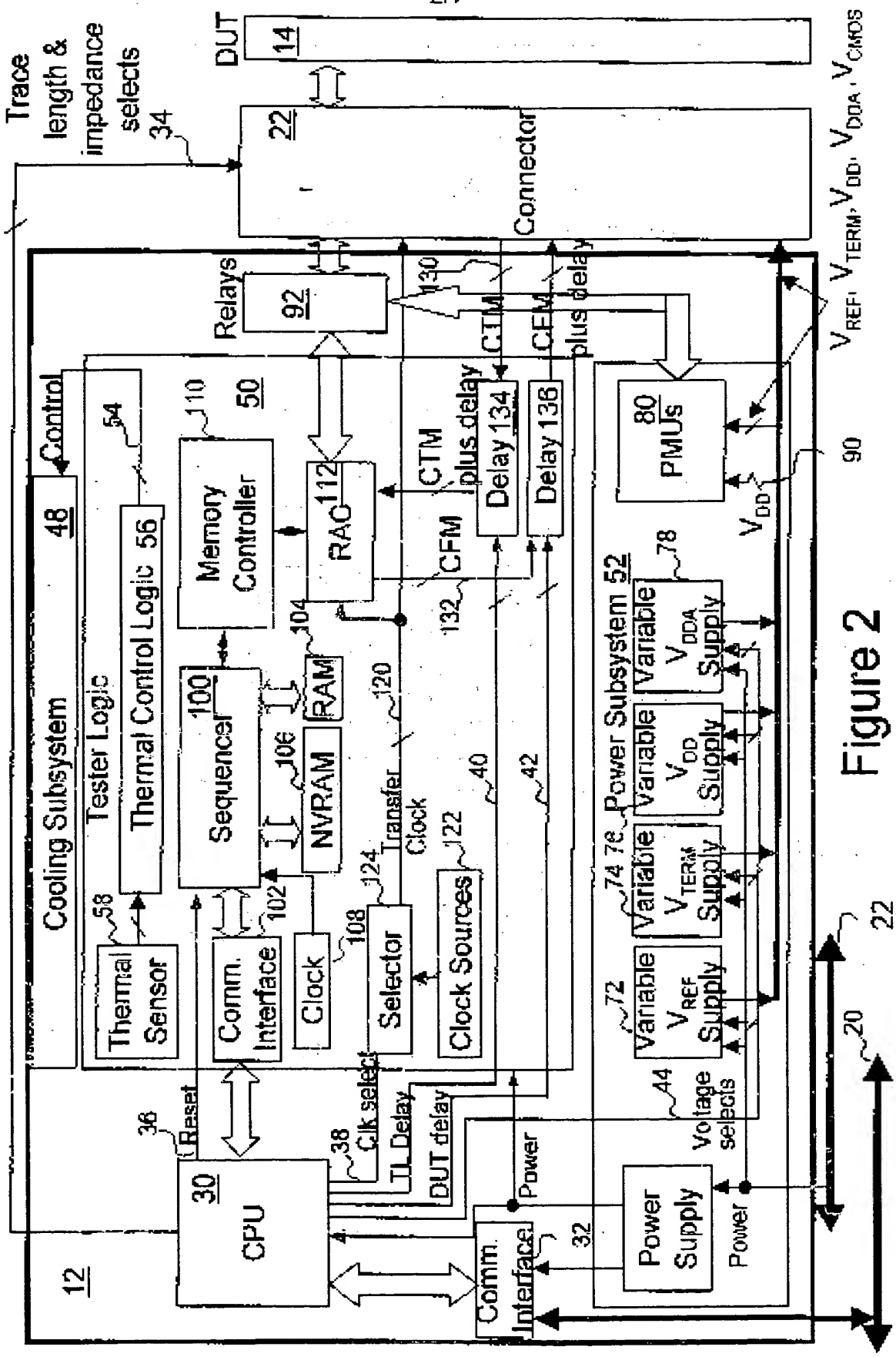

Figure 2

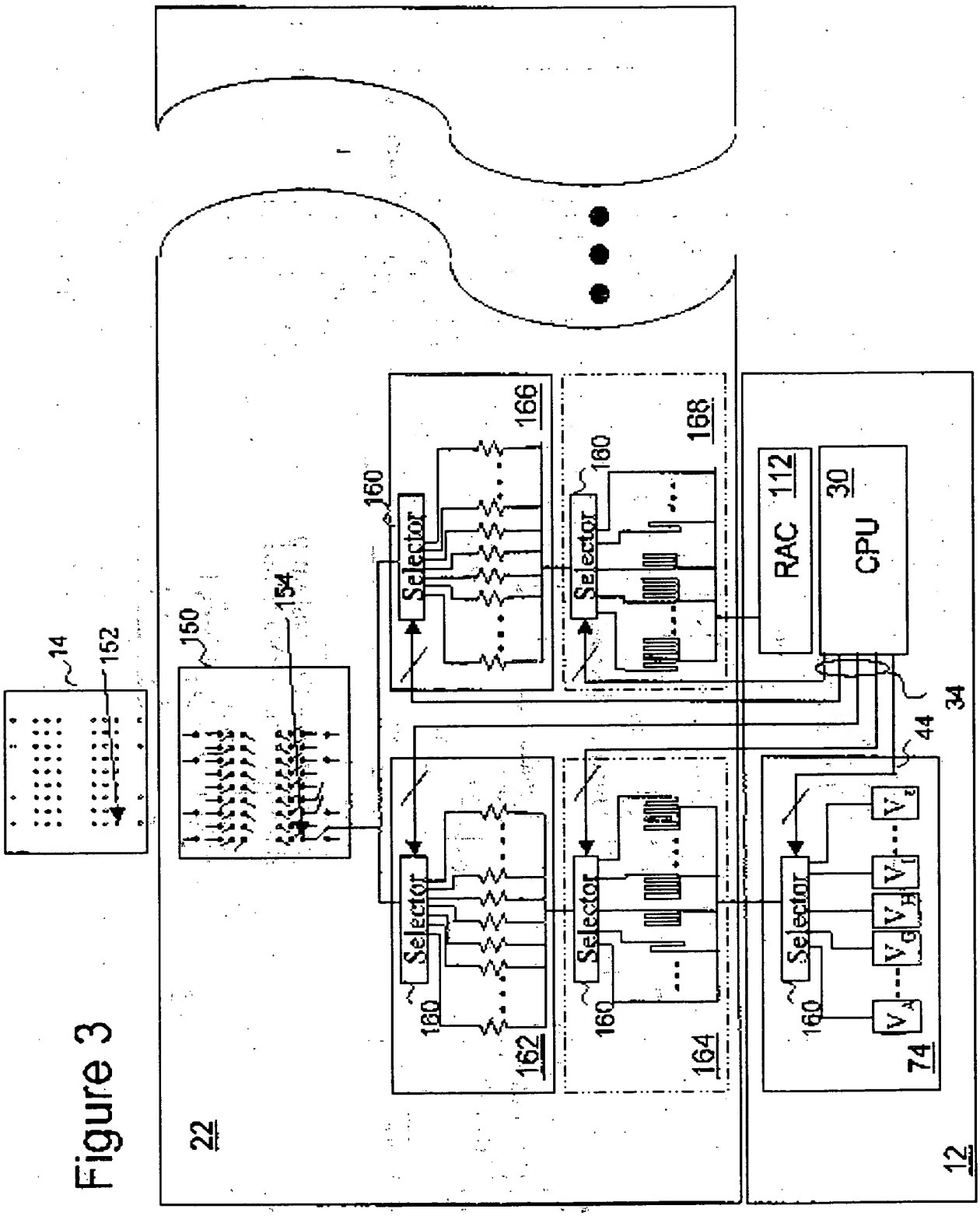

Figure 3

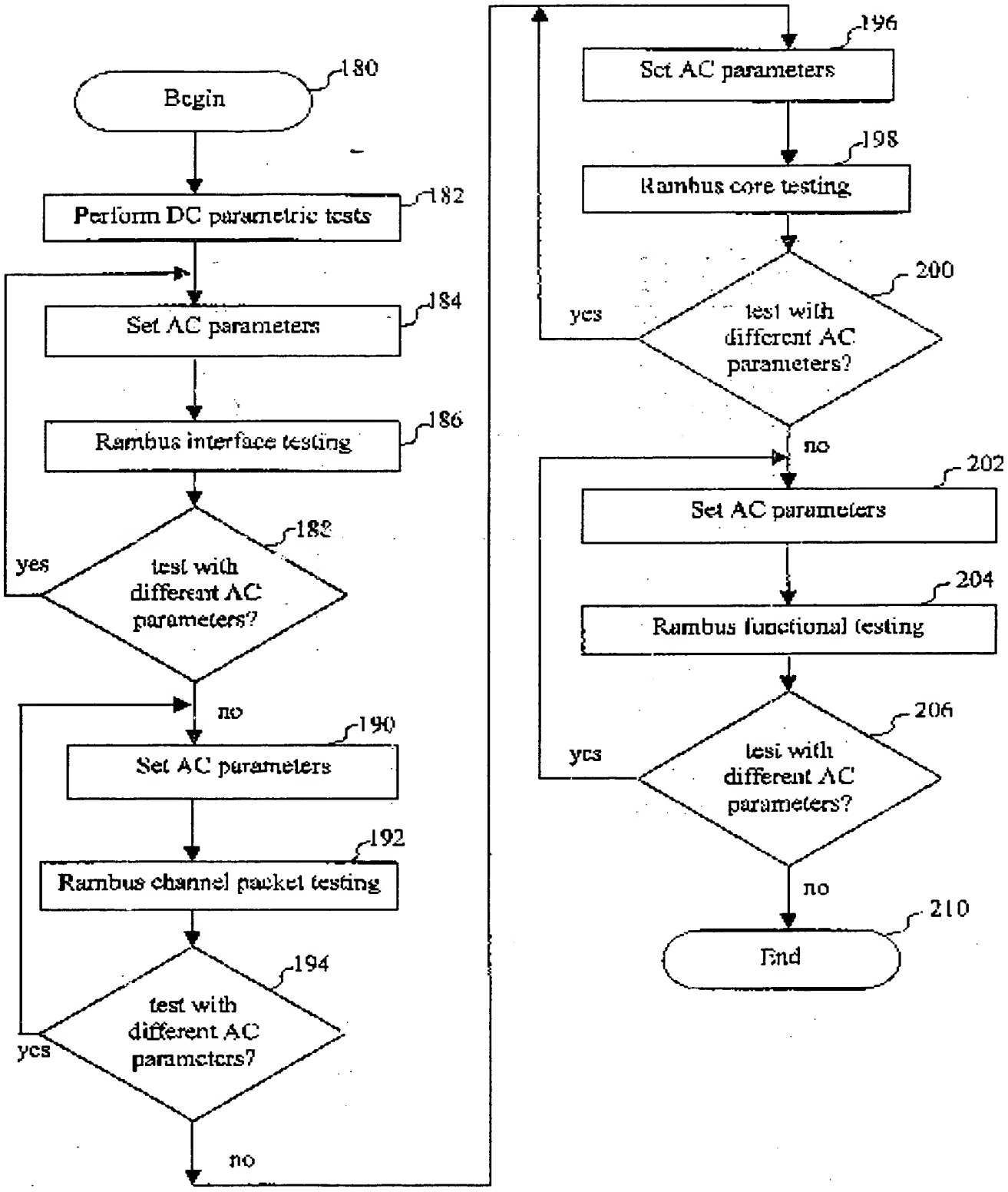

Figure 4

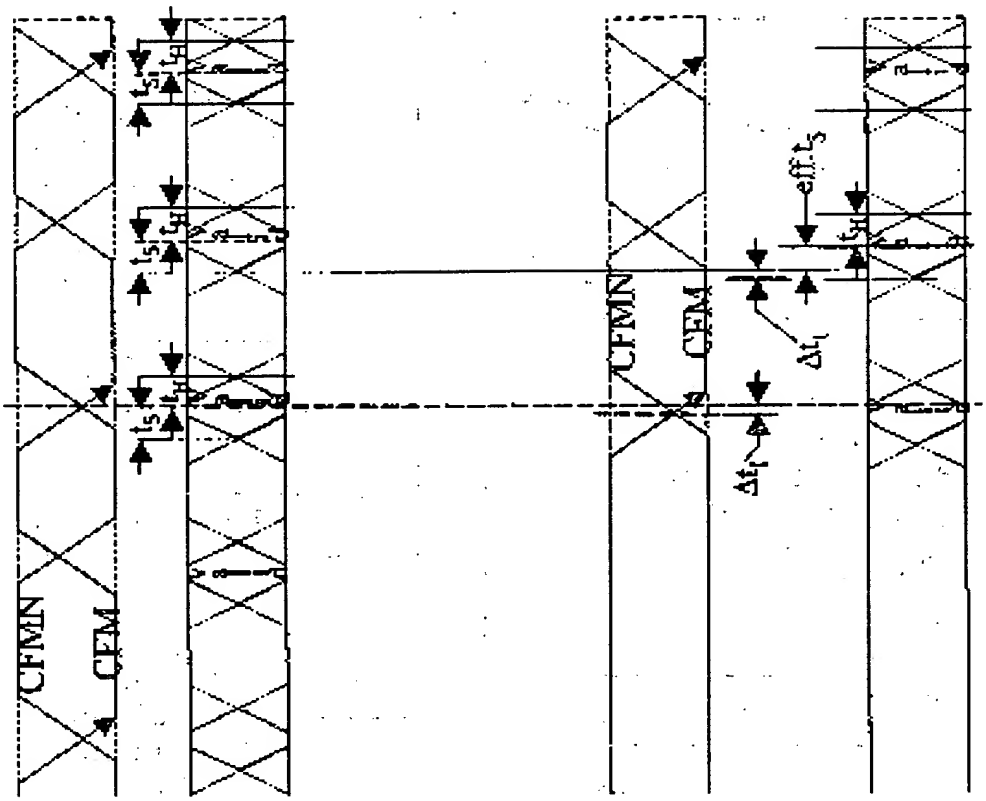

Figure 5A

Figure 5B

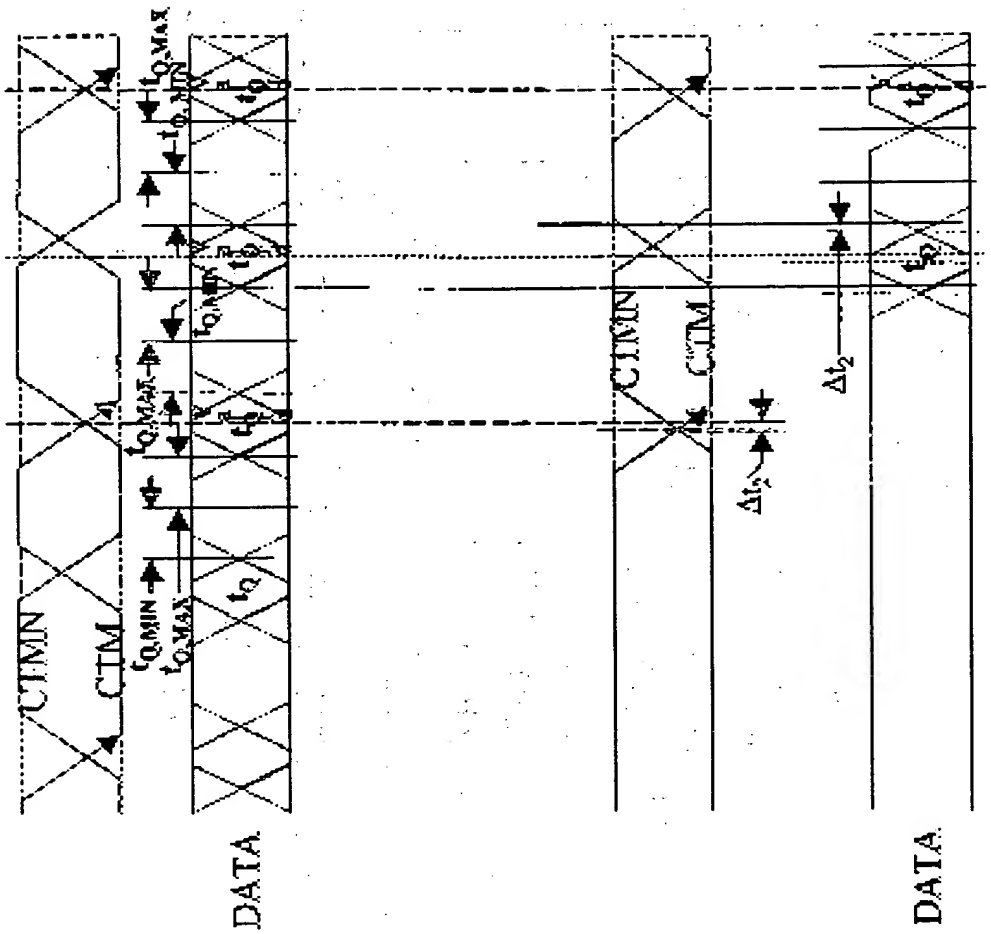

Figure 6A

Figure 6B

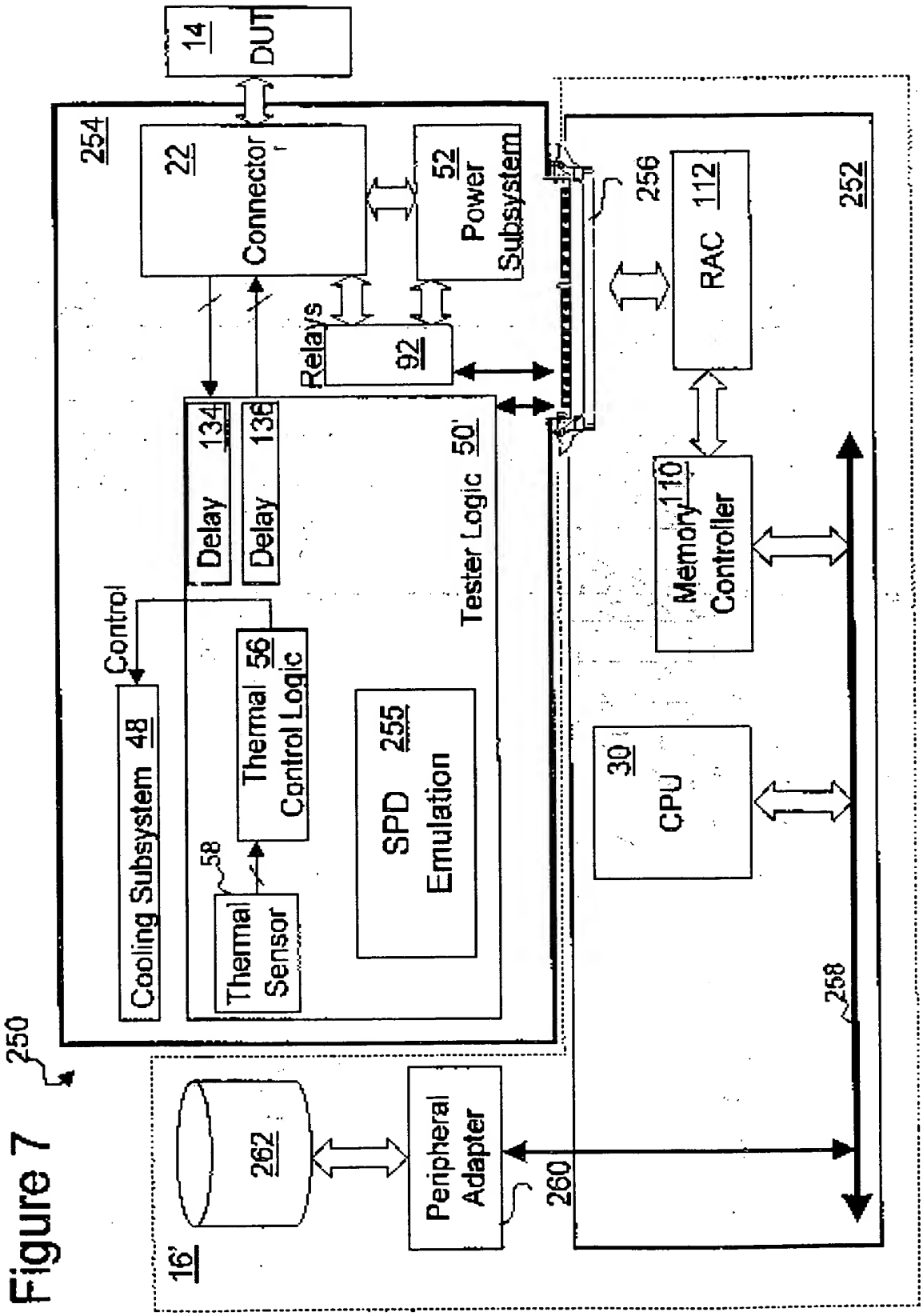

Figure 7

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GOLDBERG J M: "TIMING: THE KEY TO RAMBUS TESTING" TEST AND MEASUREMENT WORLD. (INC. ELECTRONICS TEST),US,CAHNERS PUBLISHING, DENVER, vol. 17, no. 11, 1 October 1997 (1997-10-01), pages 53-54,56,58-59, XP000725991 ISSN: 0744-1657 page 53, right-hand column, line 13-29 ---	1-3,7, 24-28, 48-54,56
A	POINTL P: "INTERFACING, OFTEN A PERFORMANCE BOTTLENECK BETWEEN ATE AND DEVICE UNDER TEST" PROCEEDINGS OF THE EUROPEAN TEST CONFERENCE,US,WASHINGTON, IEEE COMP. SOC. PRESS, vol. CONF. 1, 12 April 1989 (1989-04-12), pages 94-99, XP000044375 page 95, right-hand column, line 14-19 ---	1-3,7, 24,25
A	HO C C: "Defining tomorrow's memory module tester" E E: EVALUATION ENGINEERING,XX,XX, vol. 38, no. 3, March 1999 (1999-03), pages 14-18, XP002122524 ISSN: 0149-0370 figure 3 ---	8,32,57
Y	US 5 325 053 A (HOROWITZ MARK A ET AL) 28 June 1994 (1994-06-28) abstract; claim 1; figure 5 -----	9-15, 33-39, 58-63

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intern: al Application No
PCT/US 00/30372

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5325053 A	28-06-1994	US 5268639 A	07-12-1993
		US 5357195 A	18-10-1994

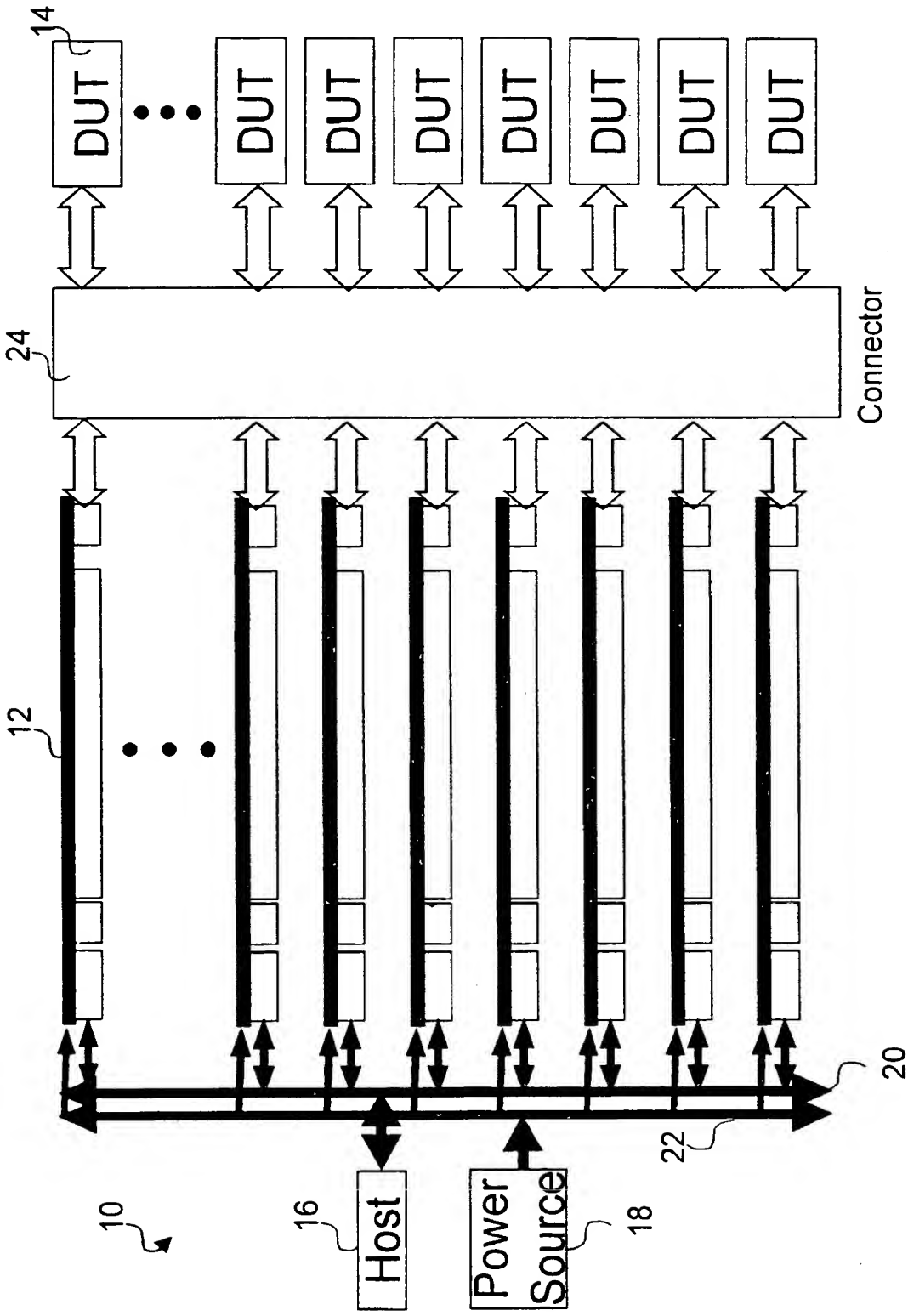

Figure 1

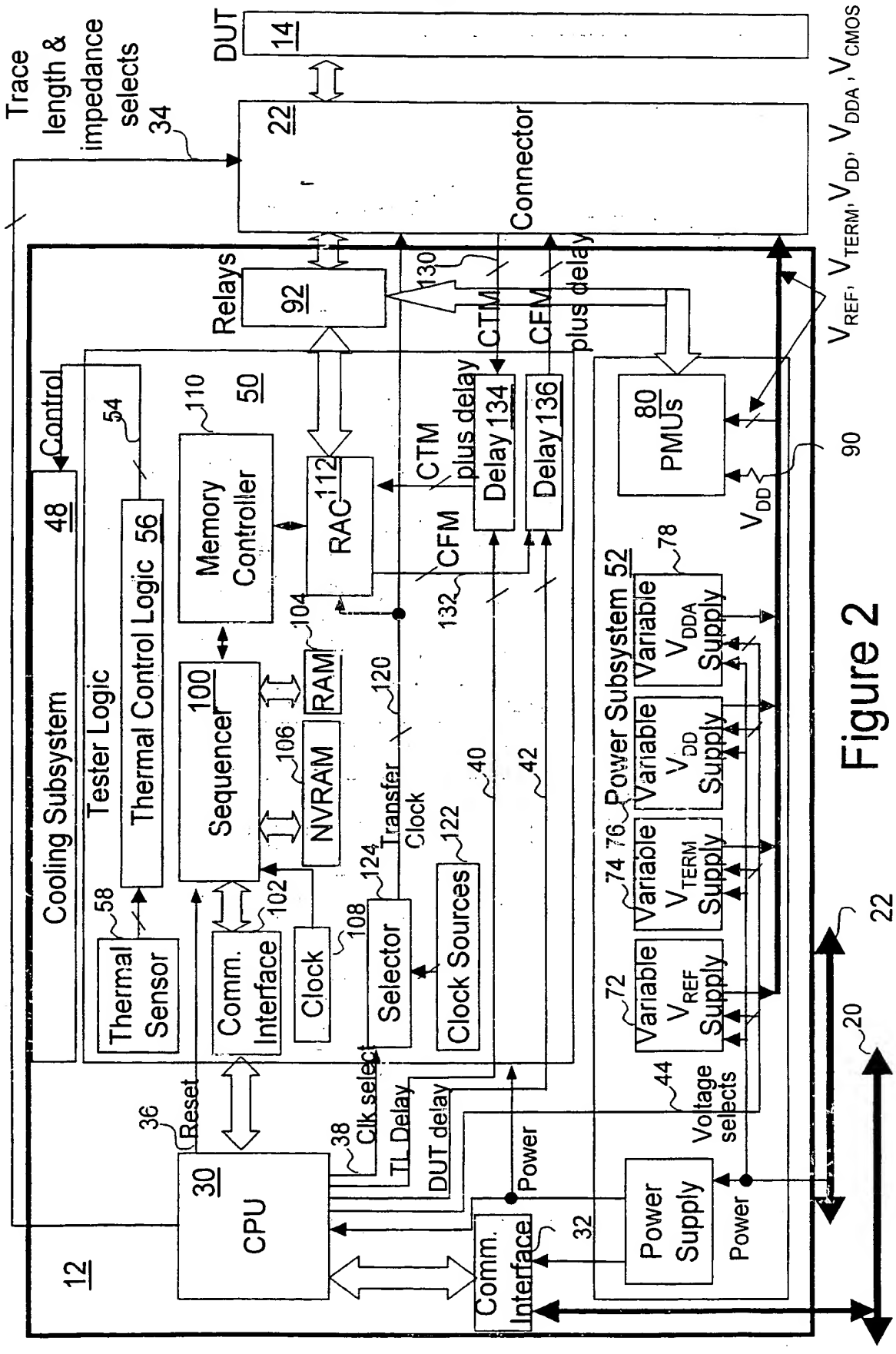
DUT
14
Trace length & impedance selects
34
22
Connector
Relays
92
130
CTM
CFM
plus delay
V_{REF}, V_{TERM}, V_{DD}, V_{DDA}, V_{CMOS}
Control
48
Cooling Subsystem
Tester Logic
54
Thermal Control Logic 56
Memory Controller
110
50
RAC
112
CTM plus delay
Delay 134
Delay 136
PMUs
80
90
V_{DD}
CFM
132
104
RAM
Sequencer
100
120
NVRAM
106
Transfer Clock
40
42
Power Subsystem 52
78
Variable V_{DDA} Supply
Variable V_{DD} Supply
74 76
Variable V_{TERM} Supply
Variable V_{REF} Supply
72
Thermal Sensor
58
Comm. Interface
102
Clock
108
Selector
124
Clock Sources
122
Reset
36
Clk select
38
TL Delay
DUT delay
Power
44
Voltage selects
CPU
30
12
Comm. Interface
32
Power Supply
Power
20
22

Figure 2

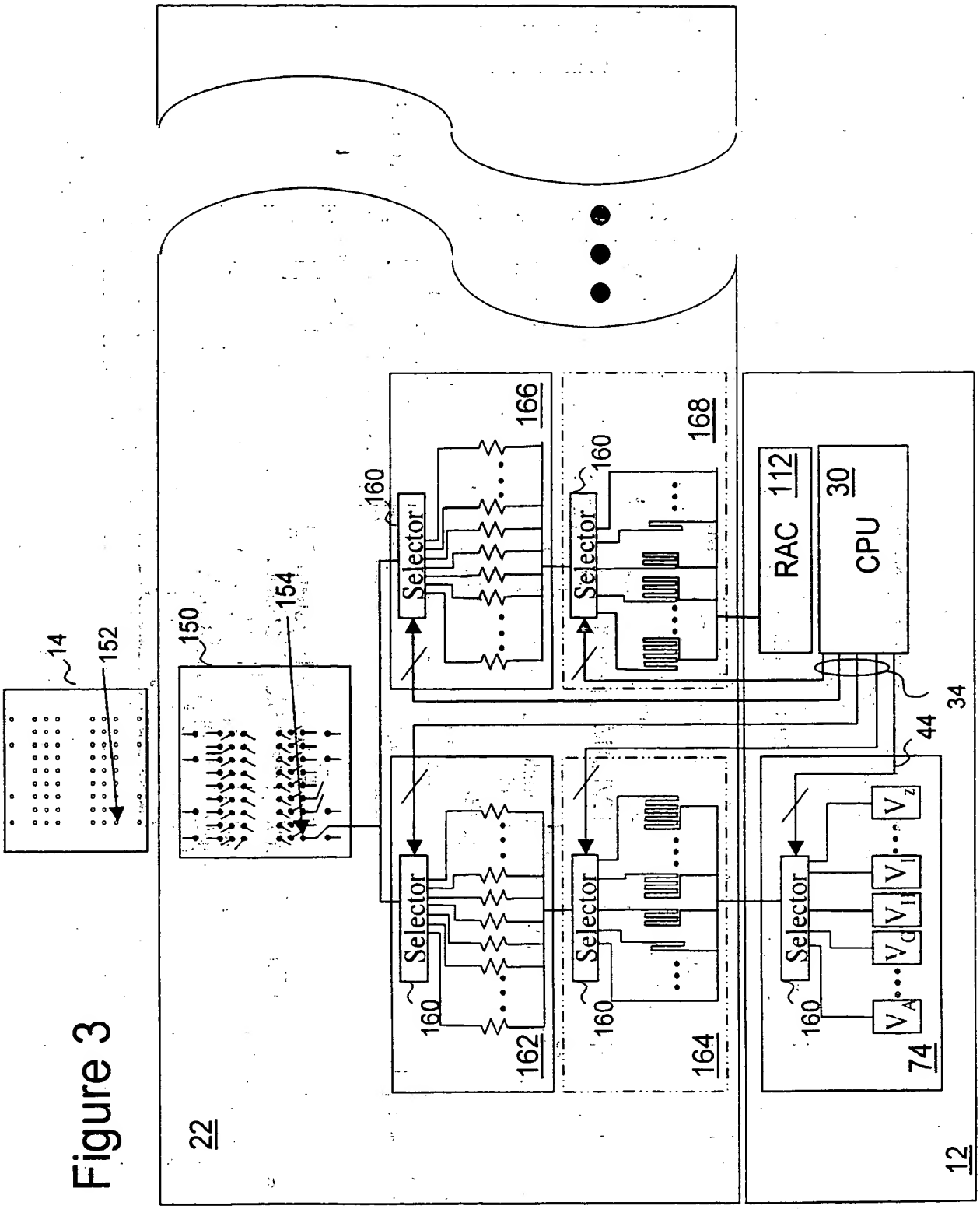

Figure 3

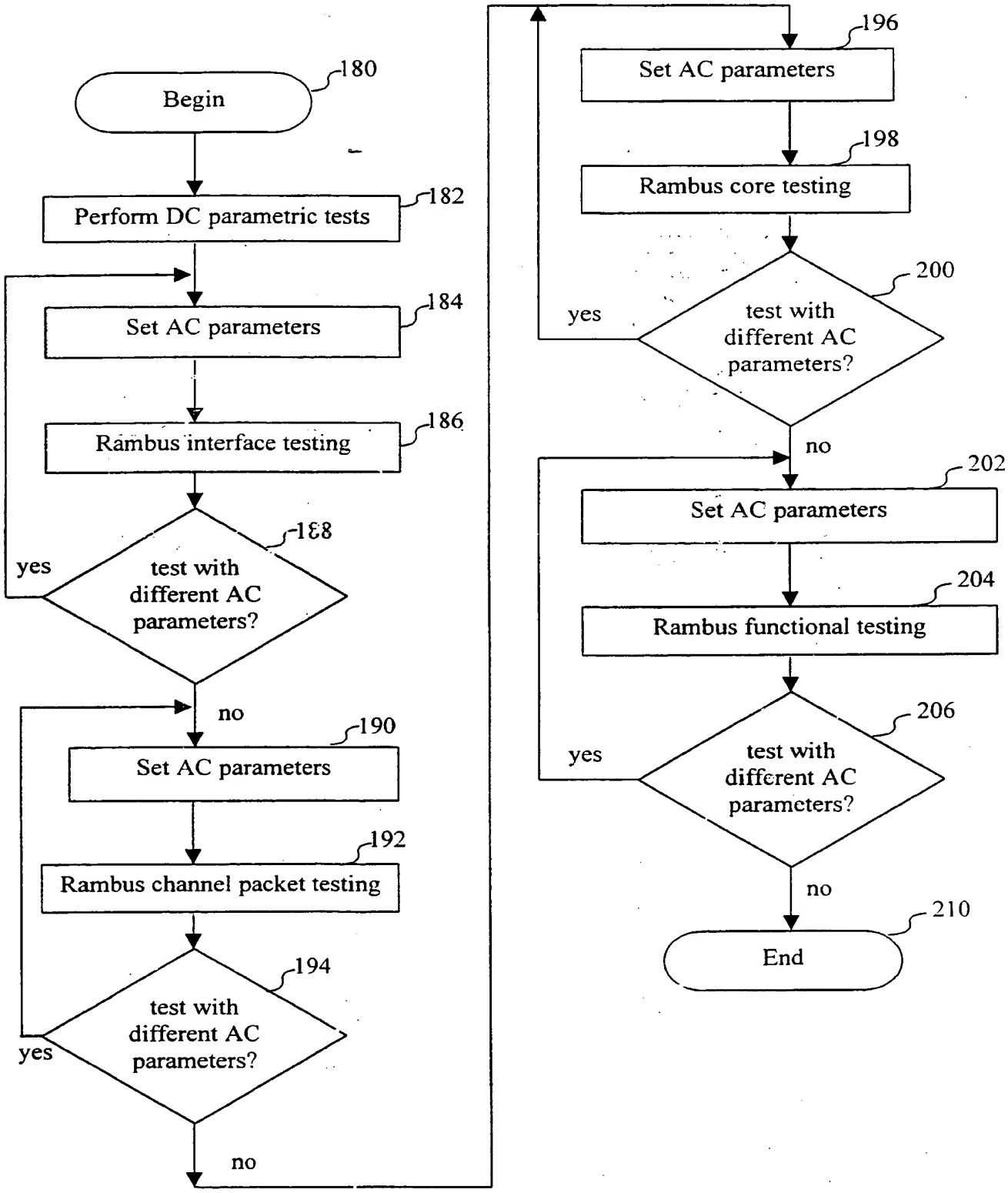

Figure 4

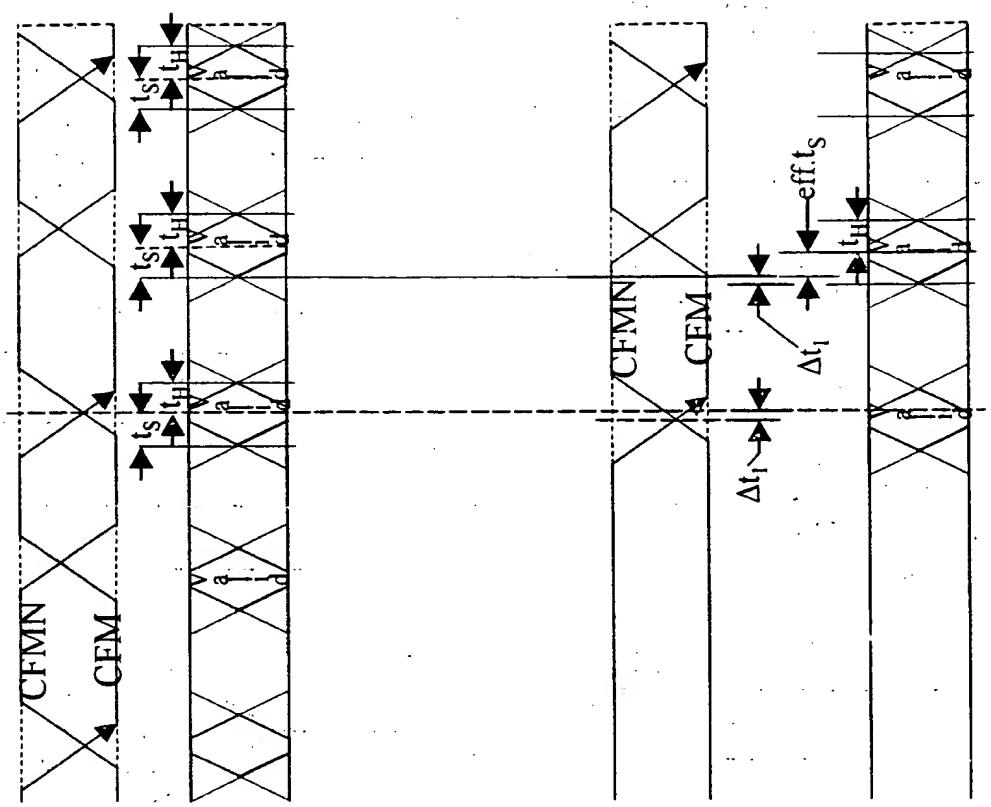

Figure 5A

Figure 5B

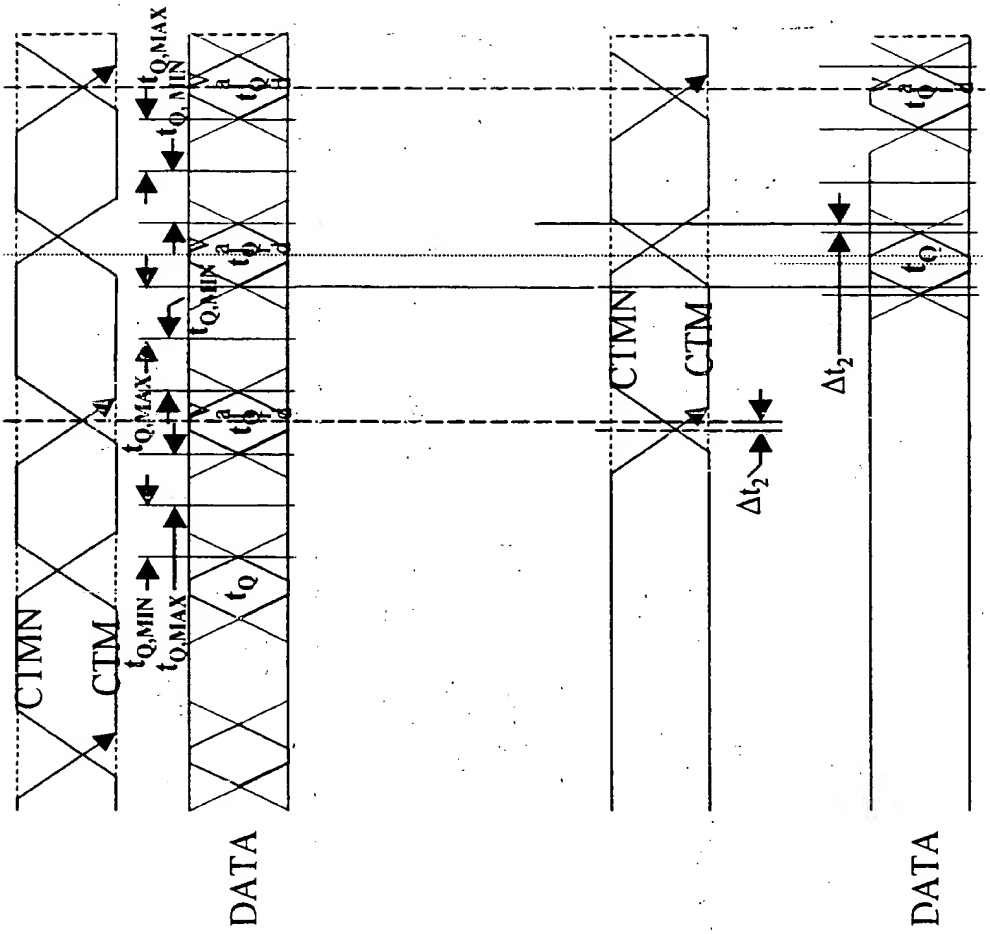

Figure 6A

Figure 6B

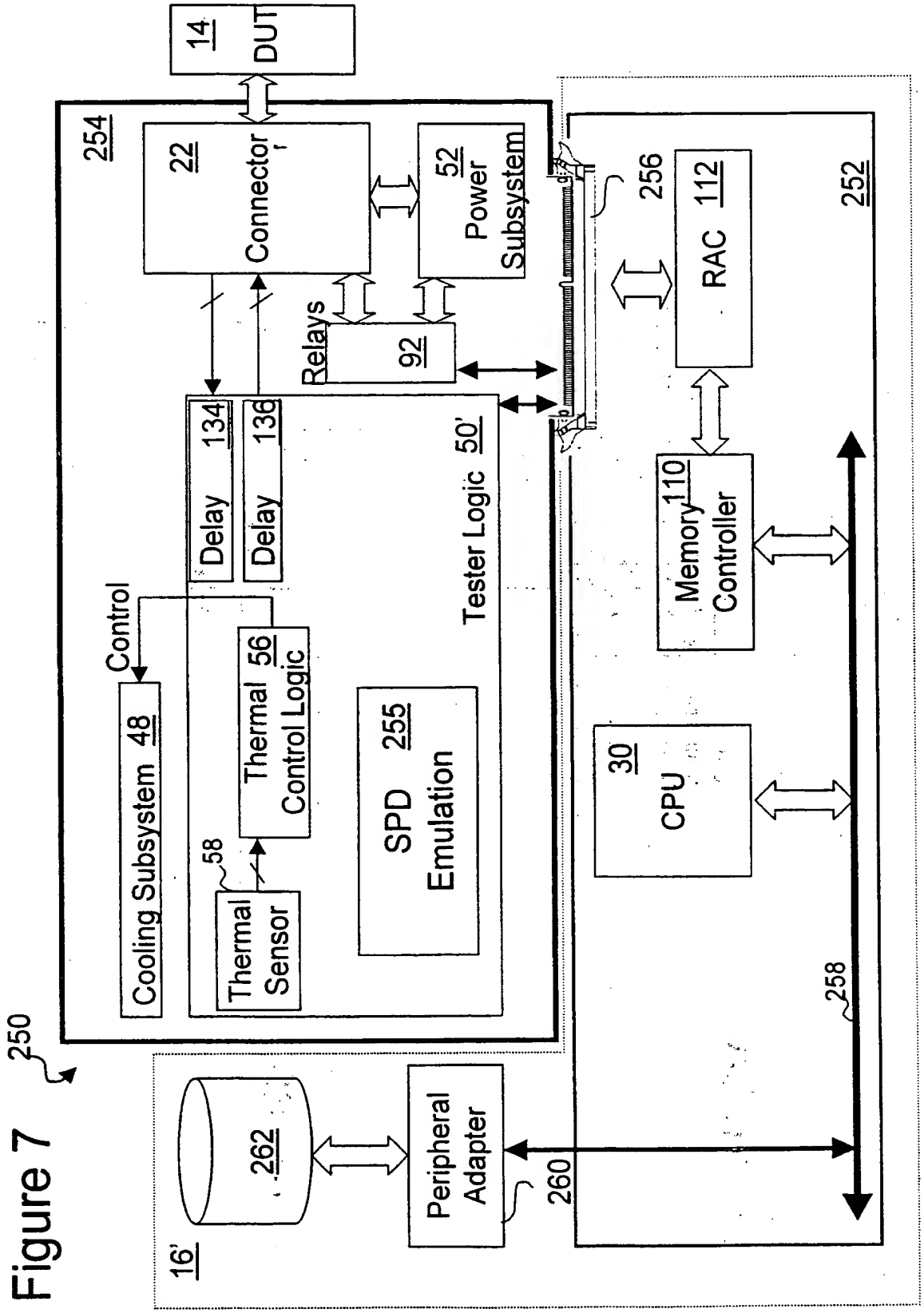

Figure 7

INTERNATIONAL SEARCH REPORT

Internal Application No
PCT/US 00/30372

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G01R31/319 G11C29/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G01R G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GASBARRO J A ET AL: "TECHNIQUES FOR CHARACTERIZING DRAMS WITH A 500 MHZ INTERFACE" PROCEEDINGS OF THE INTERNATIONAL TEST CONFERENCE,US,NEW YORK, IEEE, 2 October 1994 (1994-10-02), pages 516-525, XP000520014 ISBN: 0-7803-2103-0 page 517, right-hand column, line 15-34; figure 3	1-3,7, 24-28, 48-54,56
Y	page 518, right-hand column, line 1 -page 519, left-hand column, line 2	9-15, 33-39, 58-63

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
6 March 2001	13/03/2001

Name and mailing address of the ISA	Authorized officer
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